ABSTRACT OF THE INVENTION

A process for measuring alignment of latent images in a photoresist layer of an integrated circuit structure on a semiconductor substrate with a test pattern formed in a lower layer on the substrate comprises the steps of forming a test pattern in selected fields of a first layer on a semiconductor substrate, forming a layer of photoresist over the first layer, forming latent images in portions of the photoresist layer lying in the selected fields overlying the test pattern of the first layer; and measuring the alignment of the test pattern in the selected fields of the first layer with the overlying latent images in the photoresist layer using scatterometry. In a preferred embodiment, the test pattern formed in each of the selected fields in the first layer comprises a pattern of parallel spaced apart lines, and the latent images formed in the portions of the photoresist layer in the selected fields above the test pattern in the first layer also comprises a pattern of parallel spaced part lines, with the two sets of lines interspaced between one another and generally parallel to one another to form a diffraction pattern.